A Cirrus Logic Company

CS4390

24-Bit, Stereo D/A Converter for Digital Audio

Features

- 24-Bit Conversion
- 115 dB Signal-to-Noise-Ratio (EIAJ)
- 106 dB Dynamic Range
- -97 dB THD+N
- 128X Oversampling
- Low Clock Jitter Sensitivity
- Filtered Line-Level Outputs
  Linear Phase Filtering
  Zero Phase Error Between Channels
- Adjustable System Sampling Rates including 32kHz, 44.1kHz & 48kHz
- Digital De-emphasis for 32kHz, 44.1kHz & 48kHz
- Pin Compatible with CS4329

General Description

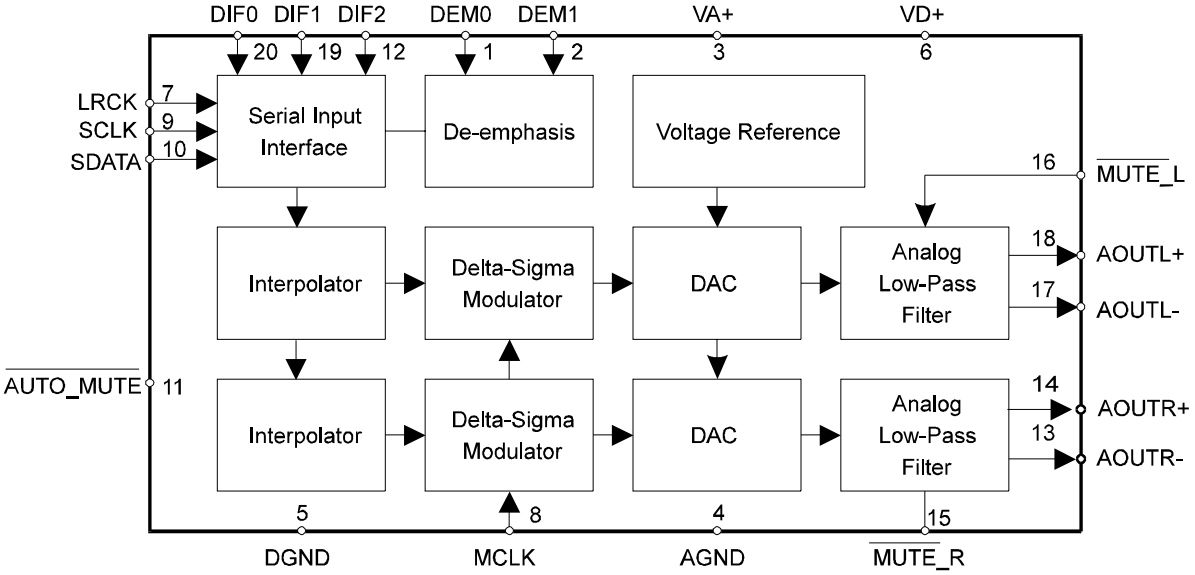
The CS4390 is a complete stereo digital-to-analog output system. In addition to the traditional D/A function, the CS4390 includes a digital interpolation filter followed by 128X oversampled delta-sigma modulator. The modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 1 and 50 kHz while maintaining linear phase response simply by changing the master clock frequency.

The CS4390 also includes an extremely flexible serial port utilizing mode select pins to support multiple interface formats.

The master clock can be either 256, 384, or 512 times the input sample rate, supporting various audio environments.

ORDERING INFORMATION:

CS4390-KP	-10 to 70 °C	20-pin Plastic DIP
CS4390-KS	-10 to 70 °C	20-pin Plastic SSOP
CDB4390	CS4390 Evaluation Board	



Preliminary Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS (T_A = 25 °C; Full-Scale Differential Output Sine wave, 997 Hz; Fs = 48 kHz; Input Data = 24 Bits; SCLK = 3.072 MHz; R_L = 20 kΩ differential; VD+ = VA+ = 5V; Logic "1" = VD+, Logic "0" = DGND; Measurement Bandwidth is 10 Hz to 20 kHz; unweighted; unless otherwise specified)

Parameter			Symbol	Min	Typ	Max	Unit
Specified Temperature Operating Range			T_A	-10	-	70	°C
Dynamic Performance							
Dynamic Range		(Note 1)					
	24-Bit			98	103	-	dB
		(A-Weighted)		101	106	-	dB
	20-Bit			-	103	-	dB
		(A-Weighted)		-	106	-	dB
	16-Bit			-	94	-	dB
		(A-Weighted)		-	96	-	dB
Total Harmonic Distortion + Noise		(Note 1)	THD+N				
	24-Bit	0 dB		TBD	-97	-	dB
		-20 dB		TBD	-83	-	dB
		-60 dB		TBD	-43	-	dB
	20-Bit	0 dB		-	-97	-	dB
		-20 dB		-	-83	-	dB
		-60 dB		-	-43	-	dB
	16-Bit	0 dB		-	-93	-	dB
		-20 dB		-	-74	-	dB
		-60 dB		-	-34	-	dB
Idle Channel Noise / Signal-to-Noise-Ratio		(Note 2)		-	115	-	dBFS
Interchannel Isolation	(1 kHz)			-	-110	-	dB
Combined Digital and Analog Filter Characteristics							
Frequency Response 10 Hz to 20 kHz		(Note 3)		-	±0.1	-	dB
Deviation from linear phase				-	±0.5	-	deg
Passband: to -0.1 dB corner		(Note 3)		0	-	21.77	kHz
Passband Ripple				-	-	±0.001	dB
StopBand		(Note 3)		26.23	-	-	kHz
StopBand Attenuation		.(Note 3)		72	-	-	dB
Group Delay				-	25/Fs	-	s
De-emphasis Error				-	-	±0.3	dB
dc Accuracy							
Interchannel Gain Mismatch				-	0.1	-	dB
Gain Error				-	±2	±5	%
Gain Drift				-	200	-	ppm/°C

Notes: 1. Triangular PDF Dithered Data

2. $\overline{\text{AUTO-MUTE}}$ active. See parameter definitions

3. The passband and stopband edges scale with frequency. For input sample rates, Fs, other than 48 kHz, the passband edge is 0.4535xFs and the stopband edge is 0.5465xFs.

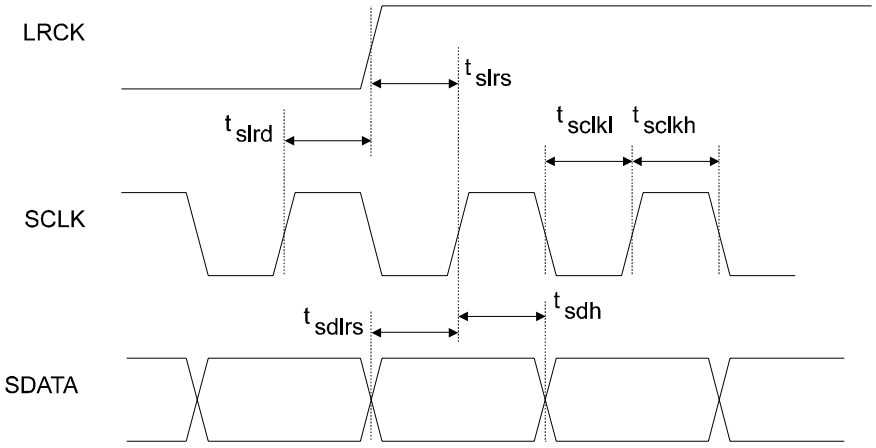
ANALOG CHARACTERISTICS (CONTINUED)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies						
Power Supply Current:	Normal Operation	IA+	-	30	-	mA
		ID+	-	12	-	mA
		(IA+) + (ID+)	-	42	50	mA
	Power-down	(IA+) + (ID+)	-	200	-	µA
Power Dissipation	Normal Operation		-	210	250	mW
	Power-down		-	1	-	mW
Power Supply Rejection Ratio (1 kHz)		PSRR	-	60	-	dB
Analog Output						
Differential Full Scale Output Voltage	(Note 4)		1.90	2.0	2.10	Vrms
Output Common Mode Voltage			-	2.2	-	V
Differential Offset			-	3	12	mV
Load Resistance			TBD	10	-	kΩ
Load Capacitance			-	-	100	pF

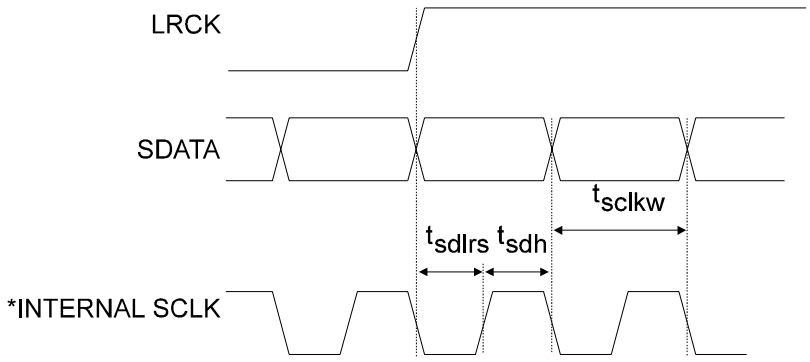
Notes: 4. Specified for a fully differential output ±((AOUT+) - (AOUT-)). See Figure 12.

SWITCHING CHARACTERISTICS (T_A = 25°C; VA+, VD+ = 5.0V; Inputs: Logic 0 = 0V, Logic 1 = VD+, C_L = 20pF))

Parameter		Symbol	Min	Typ	Max	Unit
Input Sample Rate		F_s	1	-	50	kHz
MCLK Pulse Width High	MCLK / LRCK = 512		10	-	-	ns
MCLK Pulse Width Low	MCLK / LRCK = 512		10	-	-	ns
MCLK Pulse Width High	MCLK / LRCK = 384		21	-	-	ns
MCLK Pulse Width Low	MCLK / LRCK = 384		21	-	-	ns
MCLK Pulse Width High	MCLK / LRCK = 256		31	-	-	ns
MCLK Pulse Width Low	MCLK / LRCK = 256		31	-	-	ns
External SCLK Mode						
SCLK Pulse Width Low		t_{sclkl}	20	-	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	-	ns
SCLK Period		t_{sclkw}	$\frac{1}{128(Fs)}$	-	-	ns
SCLK rising to LRCK edge delay		t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	-	ns
SDATA valid to SCLK rising setup time		t_{sdlrs}	20	-	-	ns
SCLK rising to SDATA hold time		t_{sdh}	20	-	-	ns
Internal SCLK Mode						
SCLK Period	SCLK / LRCK = 64	t_{sclkw}	$\frac{1}{64(Fs)}$	-	-	ns
SDATA valid to SCLK rising setup time		t_{sdlrs}	$\frac{1}{512(Fs)} + 10$	-	-	ns
SCLK rising to SDATA hold time	MCLK / LRCK=256 or 512	t_{sdh}	$\frac{1}{512(Fs)} + 15$	-	-	ns
SCLK rising to SDATA hold time	MCLK / LRCK = 384	t_{sdh}	$\frac{1}{384(Fs)} + 15$	-	-	ns



External Serial Mode Input Timing



Internal Serial Mode Input Timing

* The SCLK pin must be terminated to ground.
The SCLK pulses shown are internal to the CS4390.

DIGITAL CHARACTERISTICS (T_A = 25 °C; VD+ = 5V±5%)

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}	2.4	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
Input Leakage Current	V_{in}	-	-	±10.0	µA
Digital Input Capacitance		-	10	-	pF

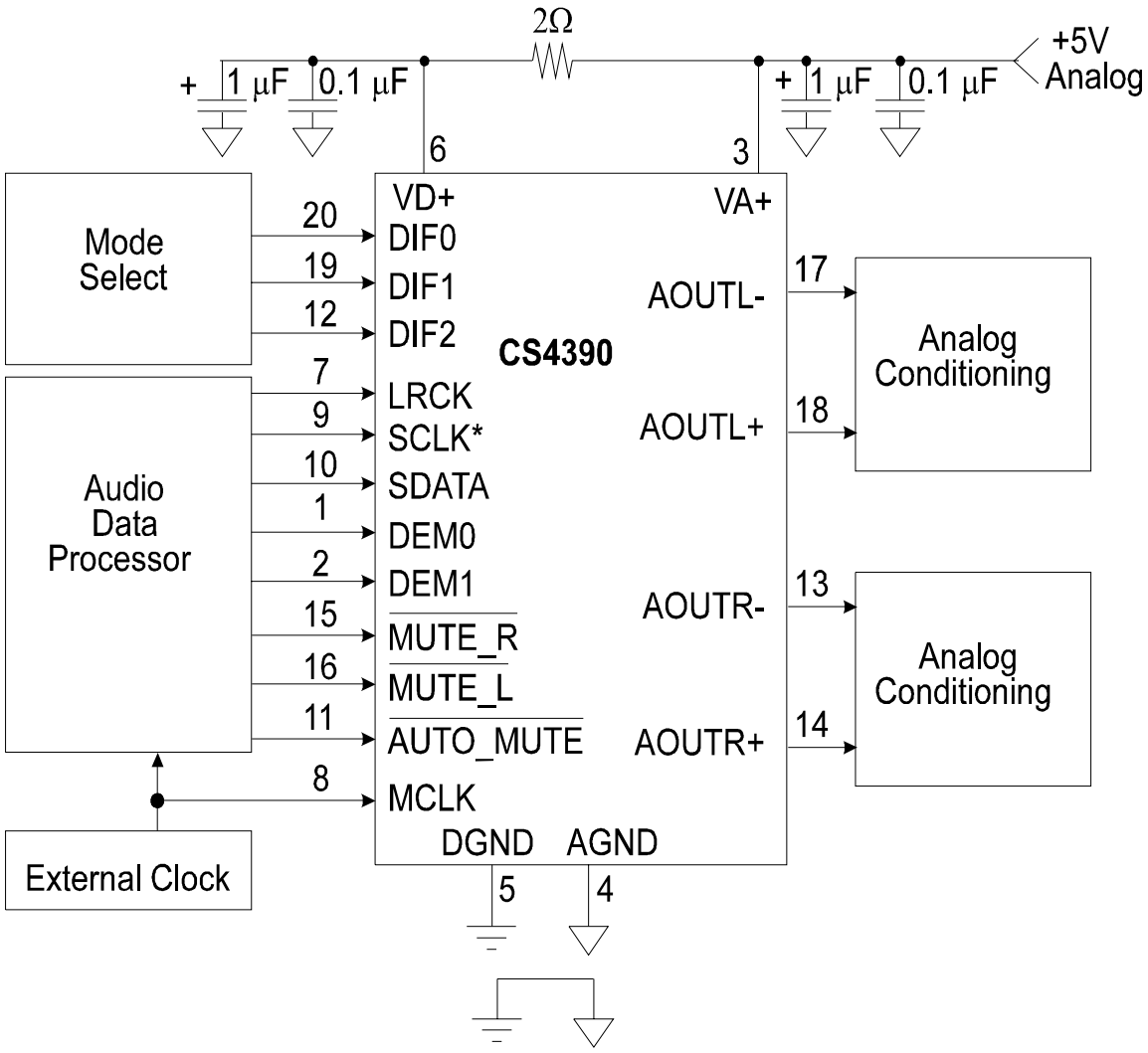
ABSOLUTE MAXIMUM RATINGS (AGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Unit
DC Power Supply:	Positive Analog	VA+	-0.3	6.0	V
	Positive Digital	VD+	-0.3	6.0	V
	|VA+ - VD+|		0.0	0.4	V
Input Current, Any Pin Except Supplies		I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	-0.3	(VD+)+0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (DGND = 0V; all voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supply:	Positive Digital	VD+	4.75	5.0	5.25	V
	Positive Analog	VA+	4.75	5.0	5.25	V
	|VA+ - VD+|		-	-	0.4	V



*SCLK must be connected to DGND for operation in Internal SCLK Mode

Figure 1. Typical Connection Diagram

GENERAL DESCRIPTION

The CS4390 is a complete stereo digital-to-analog system including 128× digital interpolation, fourth-order delta-sigma digital-to-analog conversion, 128× oversampled one-bit delta-sigma modulator and analog filtering. This architecture provides a low sensitivity to clock jitter. The DAC converts digital data at any input sample rate between 1 and 50 kHz, including the standard audio rates of 48, 44.1 and 32 kHz.

The primary purpose of using delta-sigma modulation techniques is to avoid the limitations of laser trimmed resistive DAC architectures by using an inherently linear 1-bit DAC. The advantages of a 1-bit DAC include: ideal differential linearity, no distortion mechanisms due to resistor matching errors and no linearity drift over time and temperature due to variations in resistor values.

Digital Interpolation Filter

The digital interpolation filter increases the sample rate by a factor of 4 and is followed by a 32× digital sample-and hold to effectively achieve a 128× interpolation filter. This filter eliminates images of the baseband audio signal which exist at multiples of the input sample rate, Fs. This allows for the selection of a less complex analog filter based on out-of-band noise attenuation requirements rather than anti-image filtering. Following the interpolation filter, the resulting frequency spectrum has images of the input signal at multiples of 128× the input sample rate. These images are removed by the external analog filter.

Delta-Sigma Modulator

The interpolation filter is followed by a fourth-order delta-sigma modulator which converts the interpolation filter output into 1-bit data at 128×Fs.

Switched-Capacitor DAC

The delta-sigma modulator is followed by a digital-to-analog converter which translates the 1-bit data into a series of charge packets. The magnitude of the charge in each packet is determined by sampling of a voltage reference onto a switched capacitor, where the polarity of each packet is controlled by the 1-bit signal. This technique greatly reduces the sensitivity to clock jitter and is a major improvement over earlier generations of 1-bit digital-to-analog converters where the magnitude of charge in the D-to-A process is determined by switching a current reference for a period of time defined by the master clock.

The CS4390 incorporates a differential output to maximize the output level and to minimize the amount of gain required in the output analog stage. The differential output also allows for the cancellation of common mode errors in the differential to singled-ended converter.

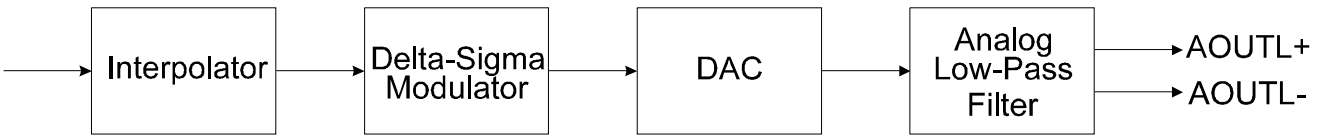


Figure 2. Block Diagram

SYSTEM DESIGN

Master Clock

The Master Clock, MCLK, is used to operate the digital interpolation filter and the delta-sigma modulator. MCLK must be either 256×, 384× or 512× the desired Input Sample Rate, Fs. Fs is the frequency at which digital audio samples for each channel are input to the DAC and is equal to the LRCK frequency. The MCLK to LRCK frequency ratio is detected automatically during the initialization sequence by counting the number of MCLK transitions during a single LRCK period. Internal dividers are then set to generate the proper clocks for the digital filter, delta-sigma modulator and switched-capacitor filter. Table 1 illustrates the standard audio sample rates and the required MCLK frequencies. Once the MCLK to LRCK frequency ratio has been detected, the phase and frequency relationship between the two clocks must remain fixed. If during any LRCK this relationship is changed, the CS4390 will reset.

Fs (kHz)	MCLK (MHz)		
	256x	384x	512x
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

Table 1. Common Clock Frequencies

Serial Data Interface

The Serial Data interface is accomplished via the serial data input, SDATA, serial data clock, SCLK, and the left/right clock, LRCK. The CS4390 supports seven serial data formats which are selected via the digital input format pins DIF0, DIF1 and DIF2. The different formats control the relationship of LRCK to the serial data and the edge of SCLK used to latch the data into the input buffer. Table 2 lists the seven formats, along with the associated figure number. The serial data is represented in 2's-complement format with the MSB-first in all seven formats.

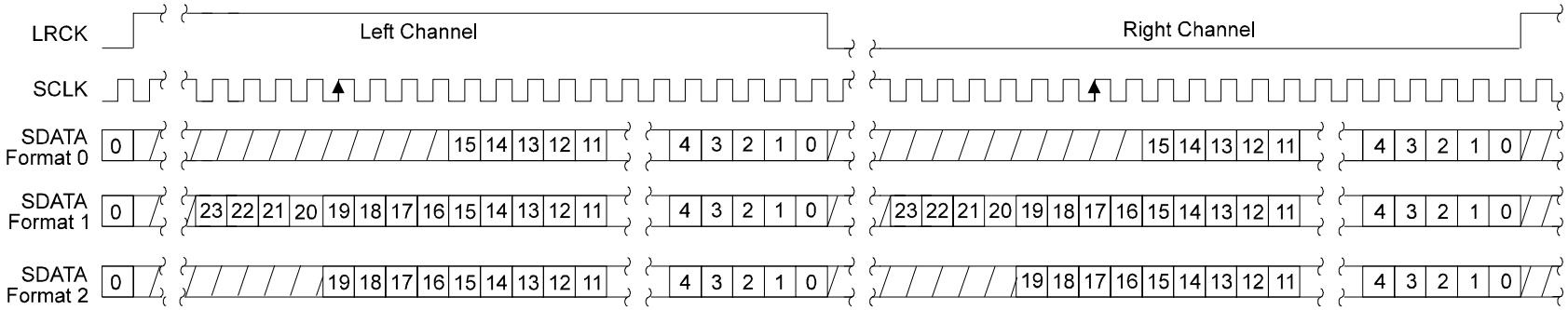
DIF2	DIF1	DIF0	Format	Figure
0	0	0	0	3
0	0	1	1	3
0	1	0	2	3
0	1	1	3	4
1	0	0	4	5
1	0	1	5	6
1	1	0	6	7
1	1	1	Calibrate	-

Table 2. Digital Input Formats

Formats 0, 1, and 2 are shown in Figure 3. The audio data is right-justified, LSB aligned with the trailing edge of LRCK, and latched into the serial input data buffer on the rising edge of SCLK. Formats 0, 1, and 2 are 16, 24, and 20-bit versions, respectively, and differ only in the number of data bits required. Format 1 in the CS4390 is not compatible with Format 1 in the CS4329.

Formats 3 and 4 are 20-bit left justified, MSB aligned with the leading edge of LRCK, and are identical with the exception of the SCLK edge used to latch data. Data is latched on the falling edge of SCLK in Format 3 and the rising edge of SCLK in Format 4. Both formats will support 16, 18, and 20-bit inputs if the data is followed by 8, 6, or 4 zeros to simulate a 24-bit input as shown in Figures 4 and 5. A very small offset will result if the 20, 18, or 16-bit data is followed by static non-zero data.

Formats 5 and 6 are compatible with the I^2S serial data protocol and are shown in Figures 6 and 7. Notice that the MSB is delayed 1 period of SCLK following the leading edge of LRCK and LRCK is inverted compared to the previous formats. Data is latched on the rising edge of SCLK. Format 5 is 16-bit I^2S while Format 6 is 24-bit I^2S. 20, 18, or 16-bit I^2S can be implemented in Format 6 if the data is followed by 4, 6, or 8 zeros respectively to simulate a 24-bit input as shown in Figure 7. A very small offset will result if the 20, 18, or 16-bit data is followed by static non-zero data.



NOTE: Format 1 is not compatible with the CS4329.

Figure 3. Digital Input Format 0, 1 and 2.

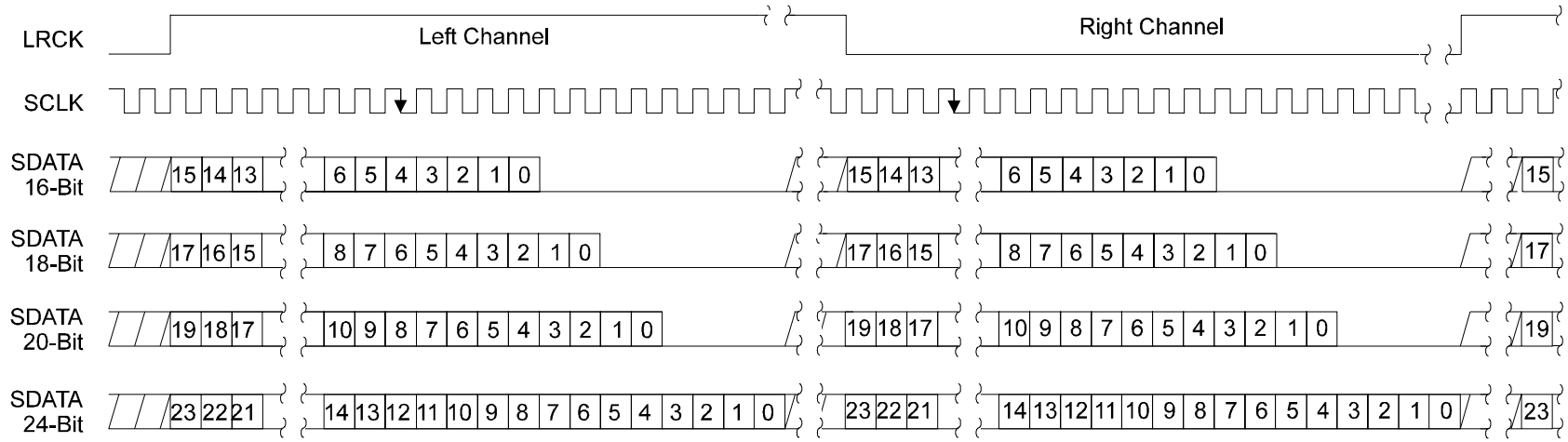


Figure 4. Digital Input Format 3.

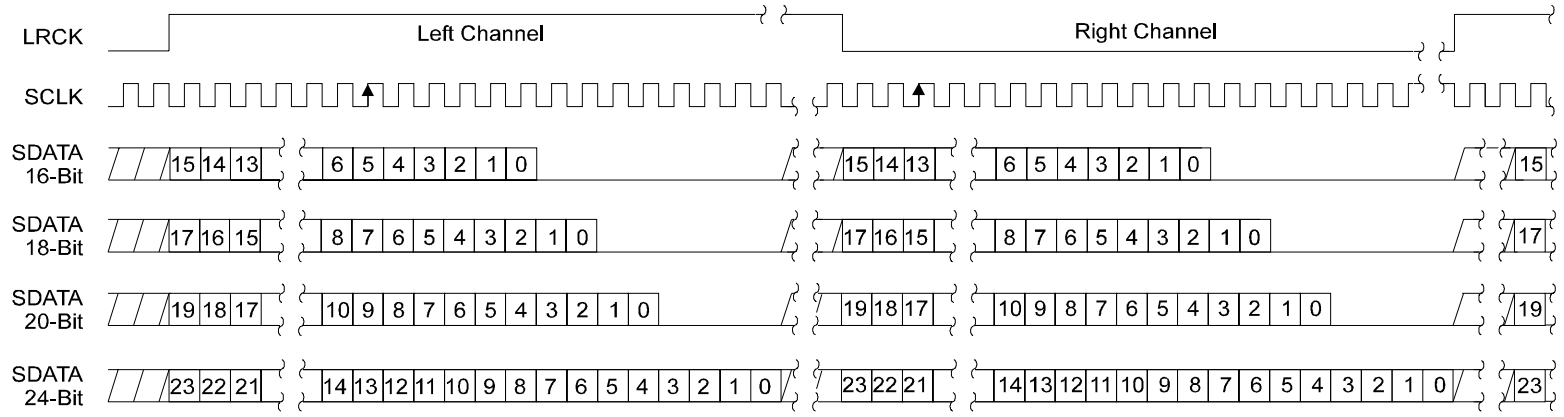


Figure 5. Digital Input Format 4.

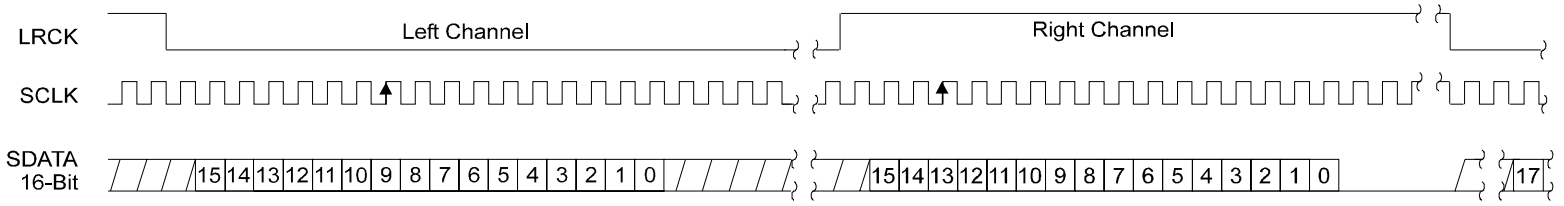


Figure 6. Digital Input Format 5.

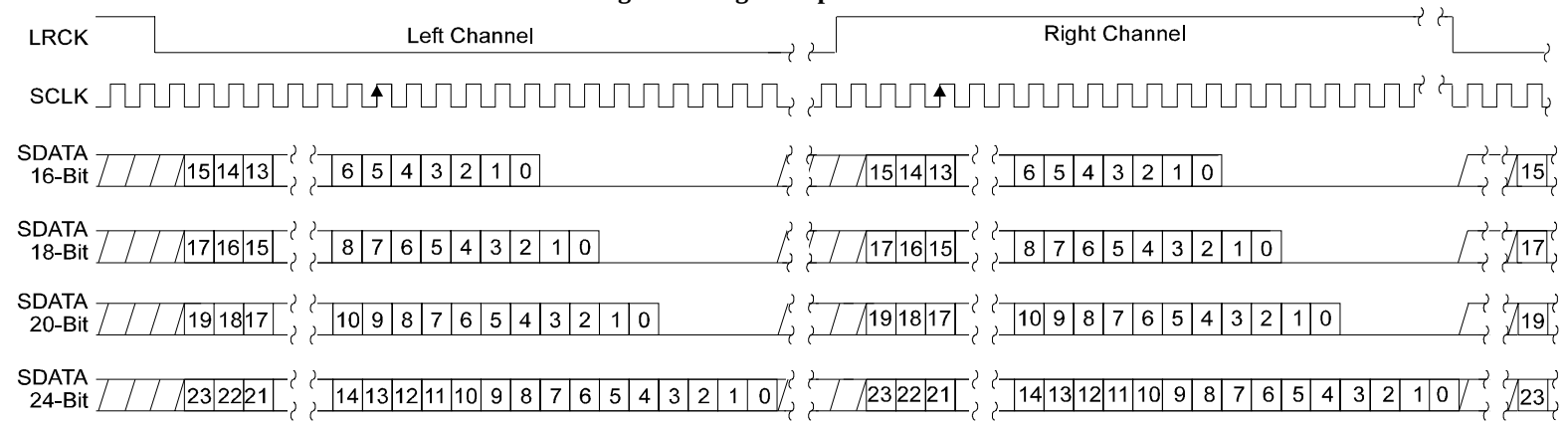


Figure 7. Digital Input Format 6.

Serial Clock

The serial clock controls the shifting of data into the input data buffers. The CS4390 supports both external and internal serial clock generation modes.

External Serial Clock

The CS4390 will enter the external serial clock mode if 15 or more high\low transitions are detected on the SCLK pin during any phase of the LRCK period. When this mode is enabled, internal serial clock mode cannot be accessed without returning to the power down mode.

Internal Serial Clock

In the Internal Serial Clock Mode, the serial clock is internally derived and synchronous with MCLK. The internal SCLK / LRCK ratio is always 64 and operation in this mode is identical to operation with an external serial clock synchronized with LRCK. The SCLK pin must be connected to DGND for proper operation.

The internal serial clock mode is advantageous in that there are situations where improper serial clock routing on the printed circuit board can degrade system performance. The use of the internal serial clock mode simplifies the routing of the printed circuit board by allowing the serial clock trace to be deleted and avoids possible interference effects.

Mute Functions

The CS4390 includes an auto-mute function which will initiate a mute if 8192 consecutive 0's or 1's are input on both the Left and Right channels. The mute will be released when non-zero input data is applied to the DAC. The auto-mute function is useful for applications, such as compact disk players, where the idle channel noise must be minimized. This feature is active only if the $\overline{\text{AUTO\_MUTE}}$ pin is low and is independent of the status of MUTE_L and MUTE_R. Either channel can also be muted instantaneously with the MUTE_L or MUTE_R.

De-Emphasis

Implementation of digital de-emphasis requires reconfiguration of the digital filter to maintain the filter response shown in Figure 8 at multiple sample rates. The CS4390 is capable of digital de-emphasis for 32, 44.1 or 48 kHz sample rates. Table 3 shows the de-emphasis control inputs for DEM 0 and DEM 1.

DEM 1	DEM 0	De-emphasis
0	0	32 kHz
0	1	44.1 kHz
1	0	48 kHz
1	1	OFF

Table 3: De-Emphasis Filter Selection

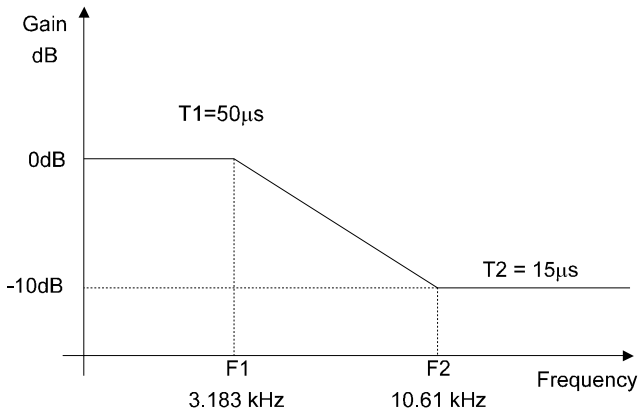


Figure 8. De-emphasis Filter Response

Initialization, Calibration and Power-Down

Upon initial power-up, the DAC enters the power-down mode. The interpolation filters and delta-sigma modulators are reset, and the internal voltage reference, one-bit D/A converters and switched-capacitor low-pass filters are powered down. The device will remain in the power-down mode until MCLK and LRCK are presented. Once MCLK and LRCK are detected, MCLK occurrences are counted over one LRCK period to determine the MCLK / LRCK frequency ratio. The phase and frequency relationship between the two clocks must remain fixed. If during any LRCK this relationship is changed, the CS4390 will reset. Power is applied to

the internal voltage reference, the D/A converters, switched-capacitor filters and the DAC will then enter a calibration mode to properly set the common mode bias voltage and minimize the differential offset. This initialization and calibration sequence requires approximately 2700 cycles of LRCK.

An offset calibration can also be invoked by taking the Format select pins, DIF0, DIF1 and DIF2, to a logic 1 as shown in Table 2. During calibration, the differential outputs are shorted together and the common-mode voltage appears at the output with approximately an 8 kohm output impedance. Following calibration, the analog output impedance becomes less than 10 ohms and the common mode voltage will move to approximately 2.2V .

The CS4390 will enter the power-down mode, within 1 period of LRCK, if either MCLK or LRCK is removed. The initialization sequence, as described above, occurs when MCLK and LRCK are restored.

Combined Digital and Analog Filter Response

The frequency response of the combined analog switched-capacitor and digital filters is shown in Figures 9, 10, and 11. The overall response is clock dependent and will scale with Fs. Note that the response plots have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs, such as 48 kHz.

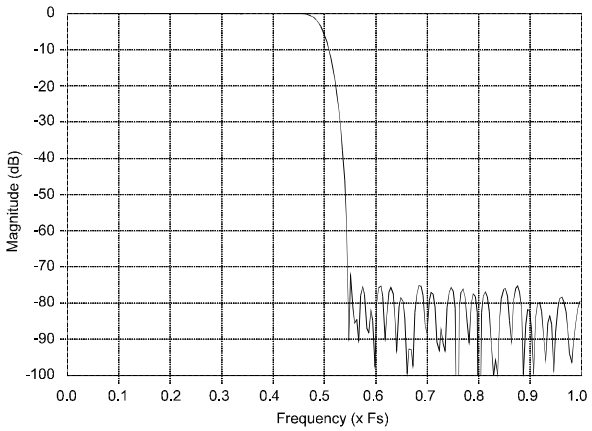


Figure 9. CS4390 Combined Digital and Analog Filter Stopband Rejection

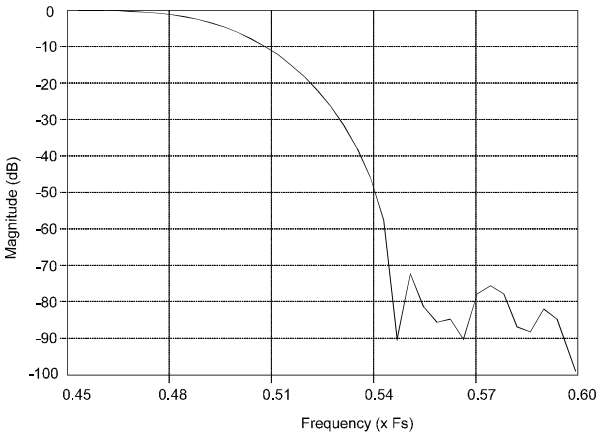


Figure 10. CS4390 Combined Digital and Analog Filter Stopband Rejection

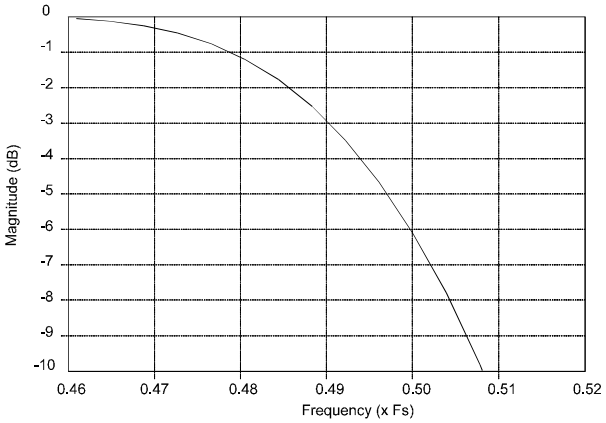


Figure 11. CS4390 Combined Digital and Analog Filter Transition Band

Analog Output and Filtering

The analog output should be operated in a differential mode which allows for the cancellation of common mode errors including noise, distortion and offset voltage. Each output will produce a nominal 2.83 Vpp (1 Vrms) output for a full scale digital input which equates to a 5.66 Vpp (2 Vrms) differential signal as shown in Figure 12.

Figure 13 displays the CS4390 output noise spectrum. The noise beyond the audio band can be further reduced with additional analog filtering. The applications note "Design Notes for a 2-Pole Filter with Differential Input " discusses the second-order Butterworth filter and differential to signal-ended converter which was implemented on the CS4390 evaluation board, CDB4390. The CS4390 filter is a linear phase design and does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response will be dependent on the external analog circuitry.

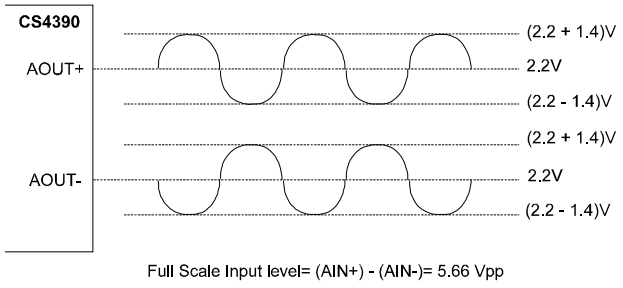


Figure 12. Full Scale Input Voltage

Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4390 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 1 shows the recommended power arrangements with VA+ connected to a clean +5 volt supply. VD+ should be derived from VA+ through a 2 ohm resistor. VD+ should not be used to power additional digital circuitry. This technique minimizes digital noise and insures proper power supply matching and sequencing. Decoupling capacitors should be located as near to the CS4390 as possible.

The printed circuit board layout should have separate analog and digital regions with individual ground planes. Extensive use of ground plane fill on both the analog and digital sections of the circuit board will yield large reductions in radiated noise effects. An application note "*Layout and Design Rules for Data Converters*" is printed in the 1994 Audio Data book.

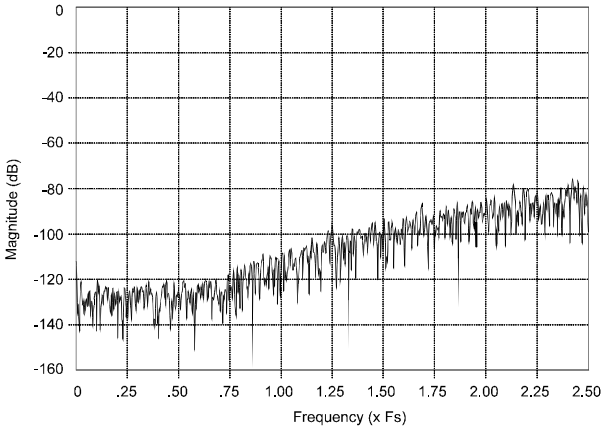
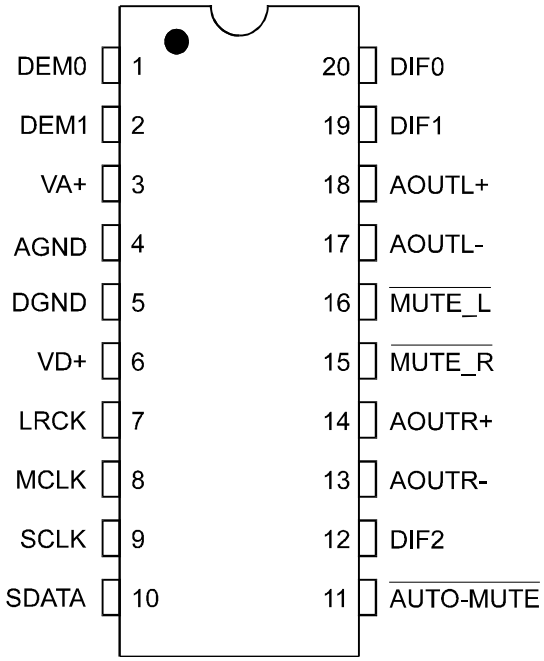


Figure 13. CS4390 Output Noise Spectrum

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, PIN 3.

Positive analog supply. Nominally +5 volts.

VD+ - Positive Digital Power, PIN 6.

Positive supply for the digital section. Nominally +5 volts.

AGND - Analog Ground, PIN 4.

Analog ground reference.

DGND - Digital Ground, PIN 5.

Digital ground for the digital section.

Analog Outputs

AOUTR+,AOUTR- - Differential Right Channel Analog Outputs, PIN 14, PIN 13.

Analog output connections for the Right channel differential outputs. Nominally 2 Vrms (differential) for full-scale digital input signal.

AOUTL+,AOUTL- - Differential Left Channel Analog Outputs, PIN 18, PIN 17.

Analog output connections for the Left channel differential outputs. Nominally 2 Vrms (differential) for full-scale digital input signal.

Digital Inputs

MCLK - Clock Input, PIN 8.

The frequency must be either 256×, 384× or 512× the input sample rate (Fs).

LRCK - Left/Right Clock, PIN 7.

This input determines which channel is currently being input on the Serial Data Input pin, SDATA. The format of LRCK is controlled by DIF0, DIF1 and DIF2.

SCLK - Serial Bit Input Clock, PIN 9.

Clocks the individual bits of the serial data in from the SDATA pin. The edge used to latch SDATA is controlled by DIF0, DIF1 and DIF2.

SDATA - Serial Data Input, PIN 10.

Two's complement MSB-first serial data of either 16, 18, 20, or 24 bits is input on this pin. The data is clocked into the CS4390 via the SCLK clock and the channel is determined by the LRCK clock. The format for the previous two clocks is determined by the Digital Input Format pins, DIF0, DIF1 and DIF2.

DIF0, DIF1, DIF2 - Digital Input Format, PINS 20, 19, 12

These three pins select one of seven formats for the incoming serial data stream. These pins set the format of the SCLK and LRCK clocks with respect to SDATA. The formats are listed in Table 2. NOTE: Format 1 is not compatible with the CS4329.

DEM0, DEM1 - De-Emphasis Select, PINS 1, 2.

Controls the activation of the standard 50/15us de-emphasis filter for either 32, 44.1 or 48 kHz sample rates.

$\overline{\text{AUTO-MUTE}}$ - Automatic Mute on Zero-Data, PIN 11.

When $\overline{\text{Auto-Mute}}$ is low the analog outputs are muted following 8192 consecutive LRCK cycles of all 0's or 1's data. Mute is canceled with the return of non-zero input data.

$\overline{\text{MUTE\_R}}$, $\overline{\text{MUTE\_L}}$ Mute, PINS 15, 16.

$\overline{\text{MUTE\_L}}$ low activates a muting function for the Left channel. $\overline{\text{MUTE\_R}}$ low activates a muting function for the Right channel.

PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFs signal. 60dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10Hz to 20kHz), including distortion components. Expressed in decibels.

Idle Channel Noise / Signal-to-Noise-Ratio

The ratio of the rms analog output level with 1kHz full scale digital input to the rms analog output level with all zeros into the digital input. Measured A-weighted over a 10Hz to 20kHz bandwidth. Units in decibels. This specification has been standardized by the Audio Engineering Society, AES17-1991, and referred to as Idle Channel Noise. This specification has also been standardized by the Electronic Industries Association of Japan, EIAJ CP-307, and referred to as Signal-to-Noise-Ratio.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Frequency Response

A measure of the amplitude response variation from 10Hz to 20kHz relative to the amplitude response at 1kHz. Units in decibels.

De-Emphasis Error

A measure of the difference between the ideal de-emphasis filter and the actual de-emphasis filter response. Measured from 10Hz to 20kHz. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

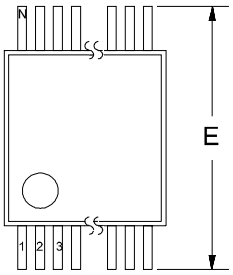
Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

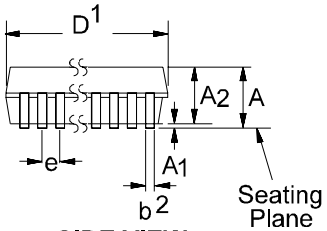
The change in gain value with temperature. Units in ppm/°C.

PACKAGE DIMENSIONS

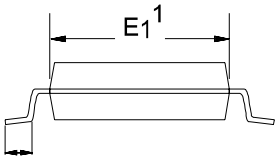


TOP VIEW

SSOP Package Dimensions



SIDE VIEW

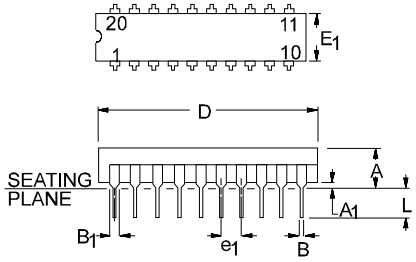


END VIEW

Notes:
1. "D" and "E_1 " are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20mm per side.
2. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13mm total in excess of b dimension at maximum material condition. Dambar intrusion shall not reduce dimension b by more than 0.07mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25mm from lead tips.

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	Note
A	-	-	2.13	-	-	0.084	
A_1	0.05	0.15	0.25	0.002	0.006	0.010	
A_2	1.62	1.75	1.88	0.064	0.070	0.074	
b	0.22	0.30	0.38	0.009	0.012	0.015	2,3
D	see other table			see other table			1
E	7.40	7.80	8.20	0.291	0.307	0.323	
E_1	5.00	5.30	5.60	0.197	0.209	0.220	1
e	0.61	0.65	0.69	0.024	0.026	0.027	
L	0.63	0.90	1.03	0.025	0.035	0.040	
N	see other table			see other table			
∝	0°	4°	8°	0°	4°	8°	

	D						
	MILLIMETERS			INCHES			
N	MIN	NOM	MAX	MIN	NOM	MAX	Note
20	6.90	7.20	7.50	0.272	0.283	0.295	1
28	9.90	10.20	10.50	0.390	0.402	0.413	1



20 pin
Plastic DIP

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	3.94	-	4.57	0.155	-	0.180
A_1	0.51	0.80	1.02	0.020	0.030	0.040
B	0.38	0.46	0.56	0.015	0.018	0.022
B_1	1.27	1.52	1.78	0.050	0.060	0.070
C	0.20	0.25	0.38	0.008	0.010	0.015
D	24.38	25.40	26.42	0.960	1.000	1.040
E_1	6.10	6.35	6.60	0.240	0.250	0.260
e_1	2.41	2.54	2.67	0.095	0.100	0.105
e_A	7.62	7.92	8.25	0.300	0.312	0.325
L	3.18	3.30	3.81	0.125	0.130	0.150
$\propto$	0°	-	15°	0°	-	15°

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION e_A TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION E_1 DOES NOT INCLUDE MOLD FLASH.

• Notes •

A Cirrus Logic Company

CDB4390

Evaluation Board for CS4390

Features

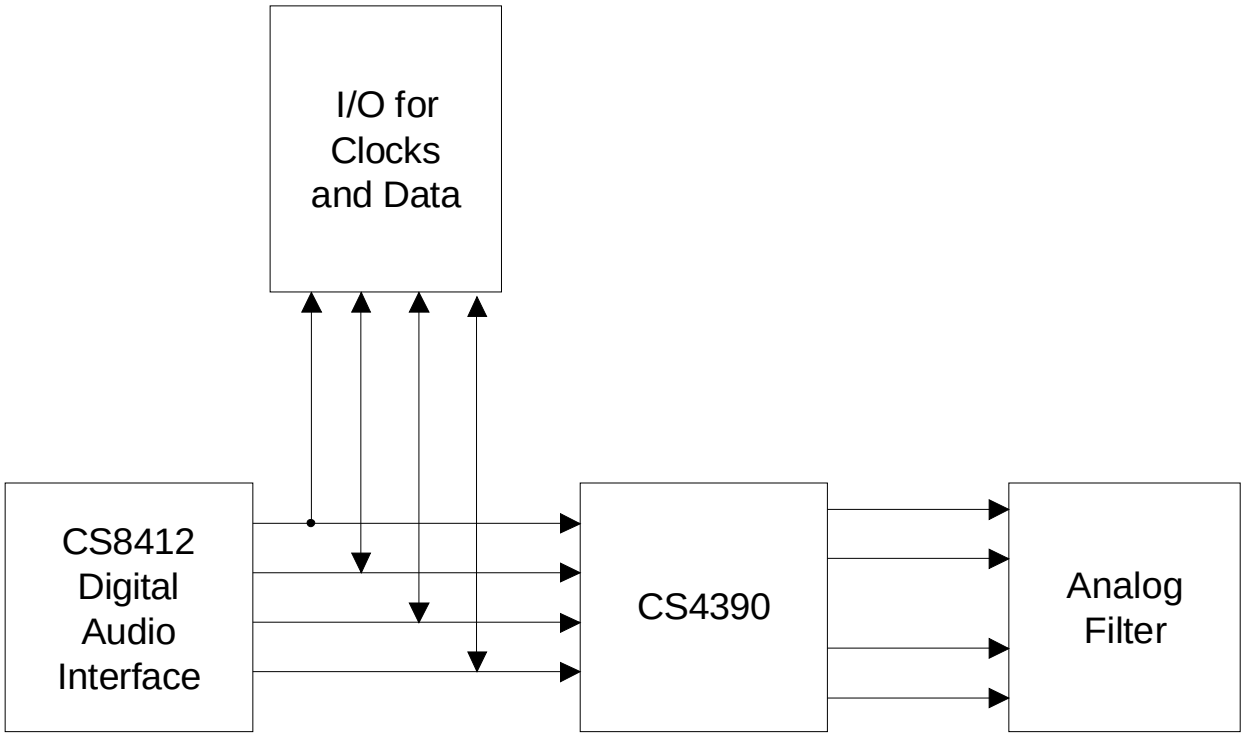
- Demonstrates recommended layout and grounding arrangements
- CS8412 Receives AES/EBU, S/PDIF, & EIAJ-340 Compatible Digital Audio
- Digital and Analog Patch Areas
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog-Converter system

Description

The CDB4390 evaluation board is an excellent means for quickly evaluating the CS4390 24-bit, stereo D/A converter. Evaluation requires an analog signal analyzer, a digital signal source and a power supply. Analog outputs are provided via RCA connectors for both channels.

The CS8412 digital audio receiver I.C. provides the system timing necessary to operate the CS4390 and will accept AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The evaluation board may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFO
CDB4390



Preliminary Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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(512) 445 7222 FAX: (512) 445 7581
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CDB4390 System Overview

The CDB4390 evaluation board is an excellent means of quickly evaluating the CS4390. The CS8412 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply clocks and data through a 10-pin header for system development.

The CDB4390 schematic has been partitioned into 8 schematics shown in Figures 2 through 9. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

CS4390 Digital to Analog Converter

A description of the CS4390 is included in the CS4390 data sheet.

CS8412 Digital Audio Receiver

The system receives and decodes the standard S/PDIF data format using a CS8412 Digital Audio Receiver, Figure 9. The outputs of the CS8412 include a serial bit clock, serial data, left-right clock (FSYNC), de-emphasis control and a 256Fs master clock. The operation of the CS8412 and a discussion of the digital audio interface are included in the 1994 *Crystal Semiconductor Audio Data Book.*

During normal operation, the CS8412 operates in the Channel Status mode where the LED's display channel status information for the channel selected by the CSLR/FCK jumper. This allows the CS8412 to decode and supply the de-emphasis bit from the digital audio interface for control of the CS4390 de-emphasis filter via pin 3, CC/F0, of the CS8412.

When the Error Information Switch is activated, the CS8412 operates in the Error and Frequency information mode. The information displayed by the LED's can be decoded by consulting the CS8412 data sheet. If the Error Information Switch is activated, the CC/F0 output has no relation to the de-emphasis bit and it is likely that the de-emphasis control for the CS4390 will be erroneous and produce an incorrect audio output.

Encoded sample frequency information can be displayed provided a proper clock is being applied to the FCK pin of the CS8412. When an LED is lit, this indicates a "1" on the corresponding pin located on the CS8412. When an LED is off, this indicates a "0" on the corresponding pin. Neither the L or R option of CSLR/FCK should be selected if the FCK pin is being driven by a clock signal.

The evaluation board has been designed such that the input can be either optical or coax, Figure 8. It is not necessary to select the active input. However, both inputs can not be driven simultaneously.

Data Format

The CS4390 must be configured to be compatible with the incoming data and can be set with DIF0, DIF1, and DIF2. The CS8412 data format can be set with the M0, M1, M2 and M3. There are several data formats which the CS8412 can produce that are compatible with CS4390. Refer to Table 2 for one possibility.

Power Supply Circuitry

Power is supplied to the evaluation board by four binding posts, Figure 10. The +5 Volt input supplies power to the CS4390 (through VA+), the CS8412 (through VA+ and VD+), and the +5 Volt digital circuitry (through VD+). The +/- 12 volt input supplies power to the analog filter circuitry.

Input/Output for Clocks and Data

The evaluation board has been designed to allow the interface to external systems via the 10-pin header, J1. This header allows the evaluation board to accept externally generated clocks and data. The schematic for the clock/data I/O is shown in Figure 7. The 74HC243 transceiver functions as an I/O buffer where the CLK SOURCE jumper deter-

mines if the transceiver operates as a transmitter or receiver.

The transceiver operates as a transmitter with the CLK SOURCE jumper in the 8412 position. LRCK, SDATA, and SCLK from the CS8412 will be available on J1. J22 must be in the 0 position and J23 must be in the 1 position for MCLK to be an output and to avoid bus contention on MCLK.

The transceiver operates as a receiver with the CLK SOURCE jumper in the EXTERNAL position. LRCK, SDATA and SCLK on J1 become inputs. The CS8412 must be removed from the evaluation board for operation in this mode.

There are 2 options for the source of MCLK in the EXT CLK source mode. MCLK can be an input with J23 in the 1 position and J22 in the 0 position. However, the recommended mode of operation is to generate MCLK on the evaluation board. MCLK becomes an output with LRCK, SCLK and SDATA inputs. This technique insures that the CS4390 receives a jitter free clock to maximize performance. This can be accomplished by installing a crystal oscillator into U4, see Figure 9 (the socket for U4 is located within the footprint for the CS8412) and placing J22 in the 1 position and J23 in the 0 position.

Analog Filter

The design of the second-order Butterworth low-pass filter, Figure 6, is discussed in the CS4390 data sheet and the applications note "Design Notes for a 2-pole Filter with Differential Input."

Grounding and Power Supply Decoupling

The CS4390 requires careful attention to power supply and grounding arrangements to optimize performance. The recommended power arrangements would be VA+ connected to a clean +5 Volt supply. The voltage VD+ (pin 6 of the CS4390) should be derived from VA+ through a 2 ohm resistor and should not used for any additional digital circuitry. Ideally, mode pins which require this voltage should be connected directly to VD+ (pin 6 of the CS4390) and mode pins which require DGND should be connected directly to pin 5 of the CS4390. AGND and DGND, Pins 4 and 5, are connected together at the CS4390. However, it was not possible to connect VD+ (pin 6 of the CS4390) and DGND to the mode pins on the CDB4390 due to layout complications resulting from the hardware selected to exercise the features of the CS4390.

Figure 2 shows the CS4390 and connections. The evaluation board has separate analog and digital regions with individual ground planes. DGND for the CS4390 should not be confused with the ground for the digital section of the system (GND). The CS4390 is positioned over the analog ground plane near the digital/analog ground plane split. These ground planes are connected elsewhere on the board. This layout technique is used to minimize digital noise and to insure proper power supply matching/sequencing. The decoupling capacitors are located as close to the CS4390 as possible. Extensive use of ground plane fill on both the analog and digital sections of the evaluation board yield large reductions in radiated noise effects.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5V	input	+5 Volts for the CS4390, CS8412 and digital section
+/- 12V	input	+/- 12 volts for analog filter section
GND	input	ground connection from power supply
Digital input	input	digital audio interface input via coax
Optical input	input	digital audio interface input via optical
J1	input/output	I/O for system clocks and digital audio data
AOUTL	output	left channel analog output
AOUTR	output	right channel analog output

Table 1. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
CSLR/FCK	Selects channel for CS8412 channel status information	L R	See CS8412 data sheet for details
Clock Select	Selects source of system clocks and data	*8412 EXT	CS8412 clock/data source External clock/data source
J22 J23	Selects MCLK as input or output	0 1	See *Input/Output for Clocks and Data* section of text
M0 M1 M2 M3	CS8412 mode select	*Low *Low *Low *Low	See CS8412 data sheet for details
auto_mute	CS4390 Auto Mute	*Low High	On Off
DEM0 DEM1	De-emphasis select	*High *Low	See CS4390 data sheet for details set for 44.1 kHz
DIF0 DIF1 DIF2	CS4390 digital input format	*High *High *Low	See CS4390 data sheet for details
SCLK	CS4390 SCLK Mode	*INT EXT	Internal SCLK Mode External SCLK Mode
DEM_8412	Selects source of de-emphasis control	*Low High	CS8412 de-emphasis De-emphasis input static high

Notes: 1. * Default setting from factory

Table 2. CDB4390 Jumper Selectable Options

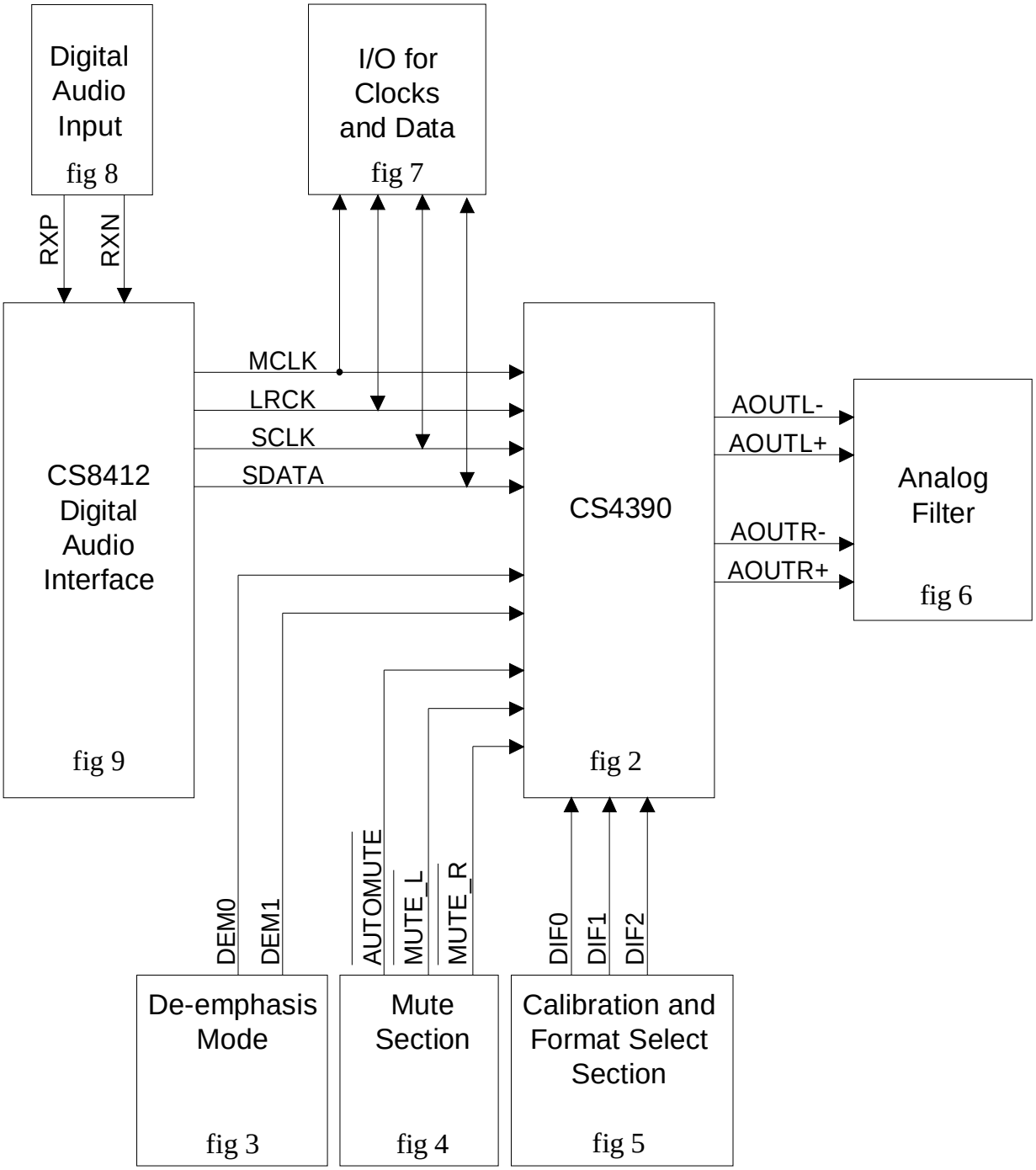


Figure 1. System Block Diagram and Signal Flow

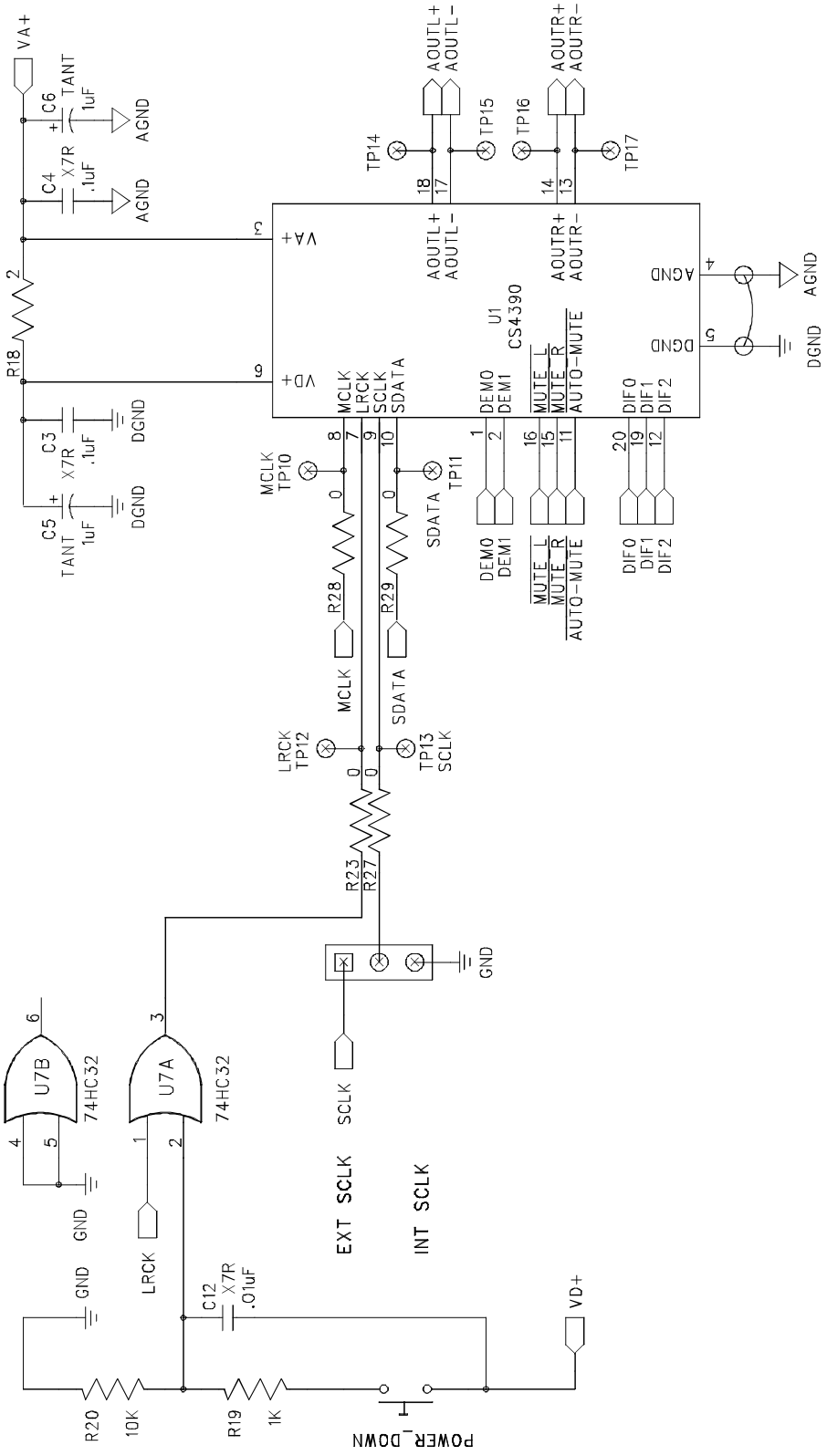


Figure 2. CS4390 and Connections

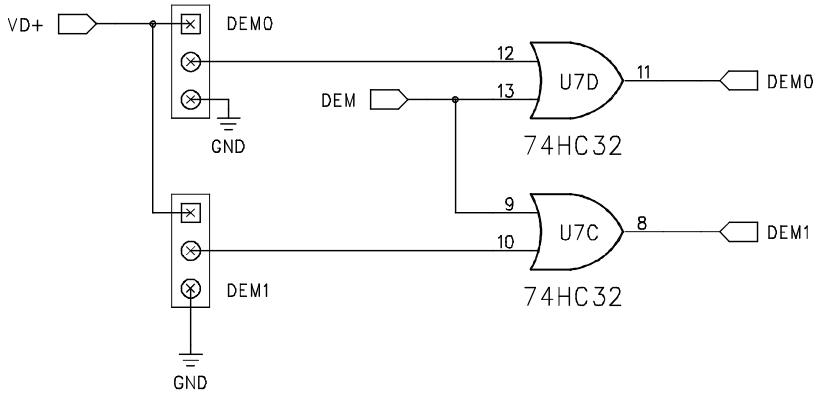


Figure 3. De-emphasis Circuitry

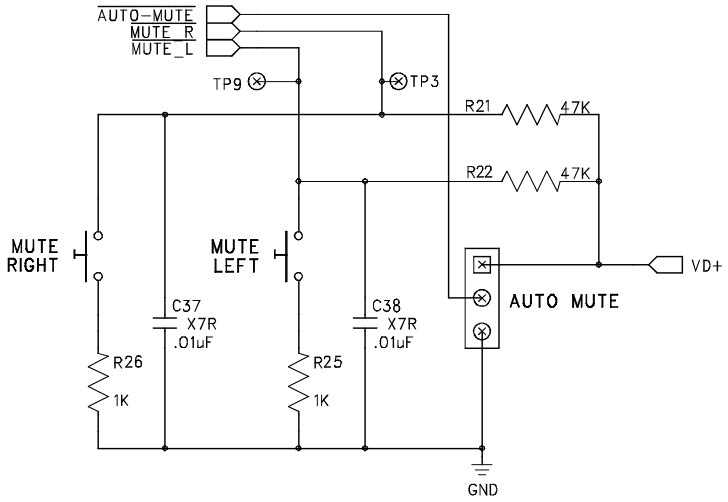


Figure 4. Mute Circuitry

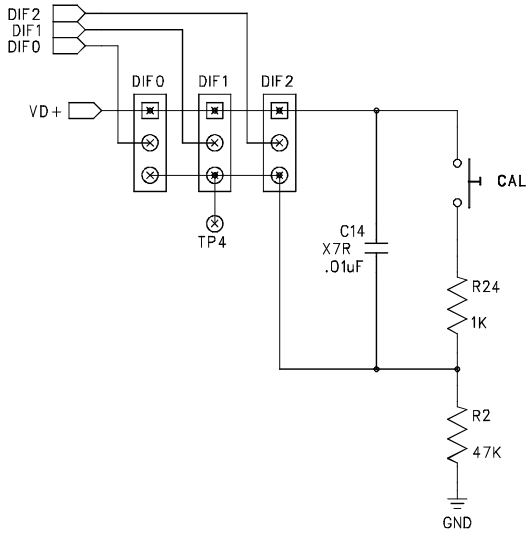
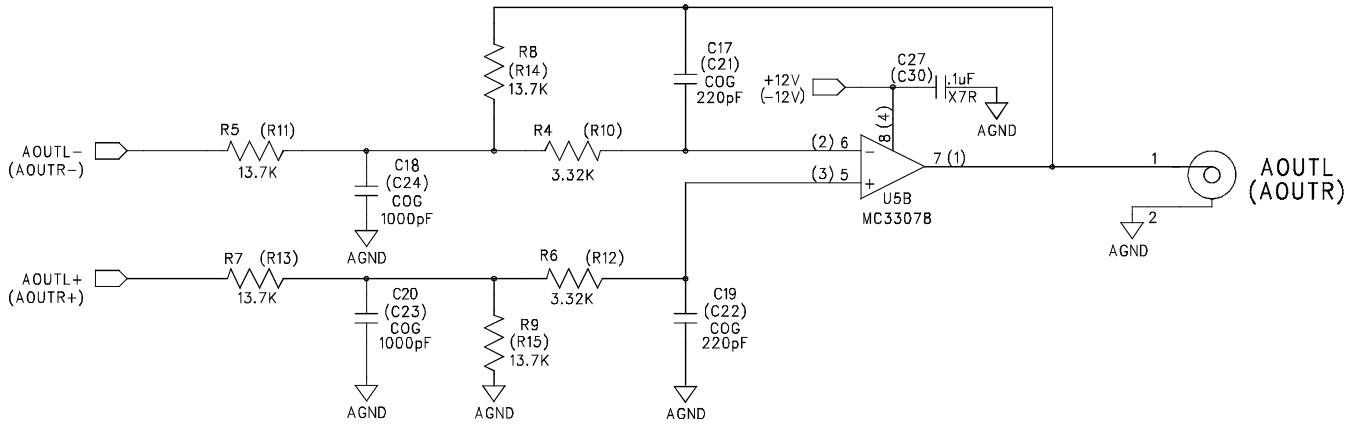


Figure 5. Calibration and Format Select Circuitry



NOTE: Right Channel components in parentheses

Figure 6. 2-pole Analog Filter

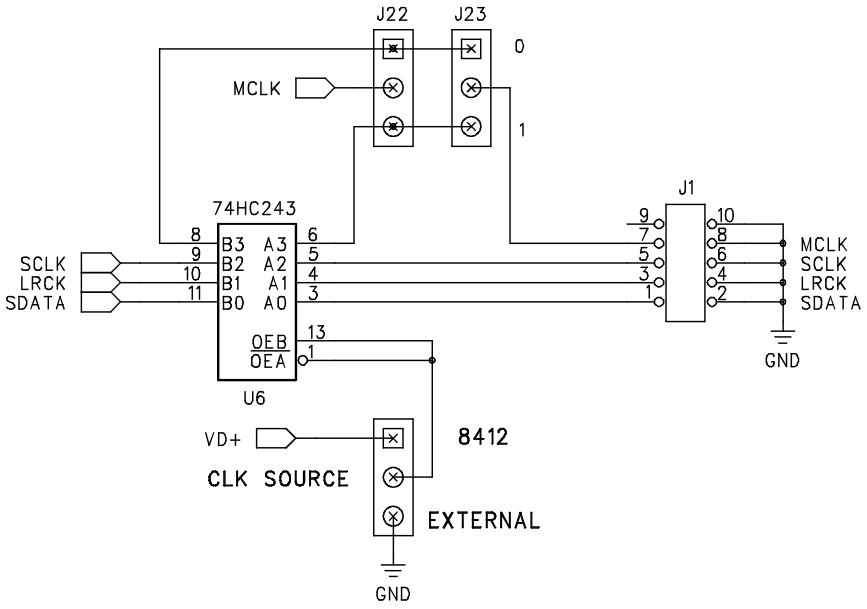
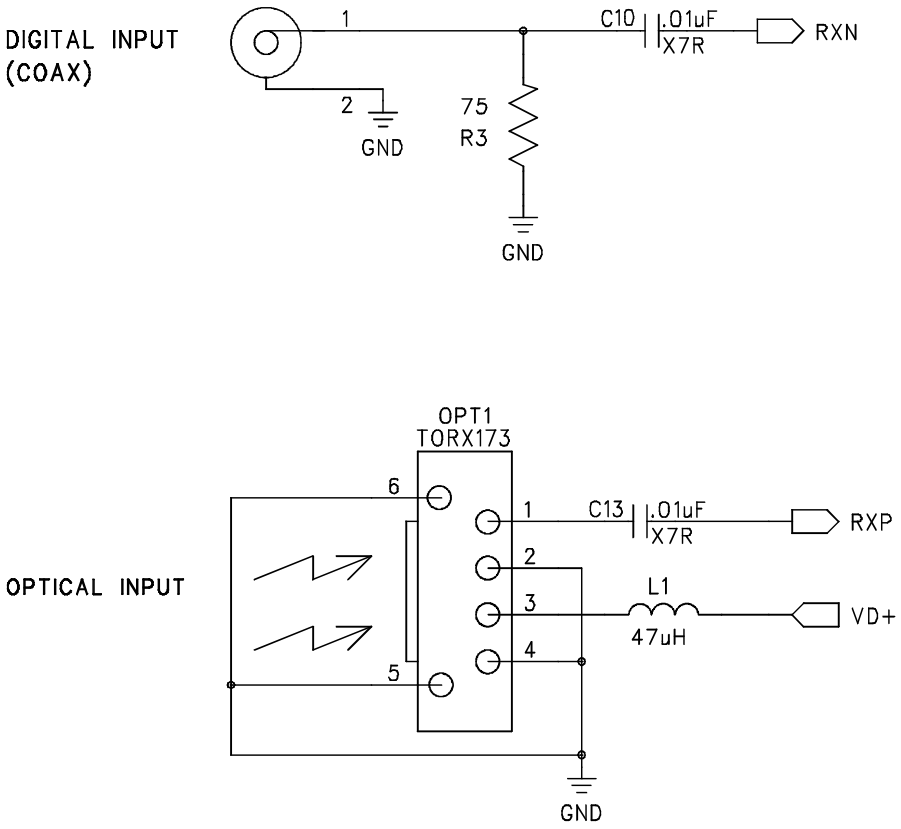
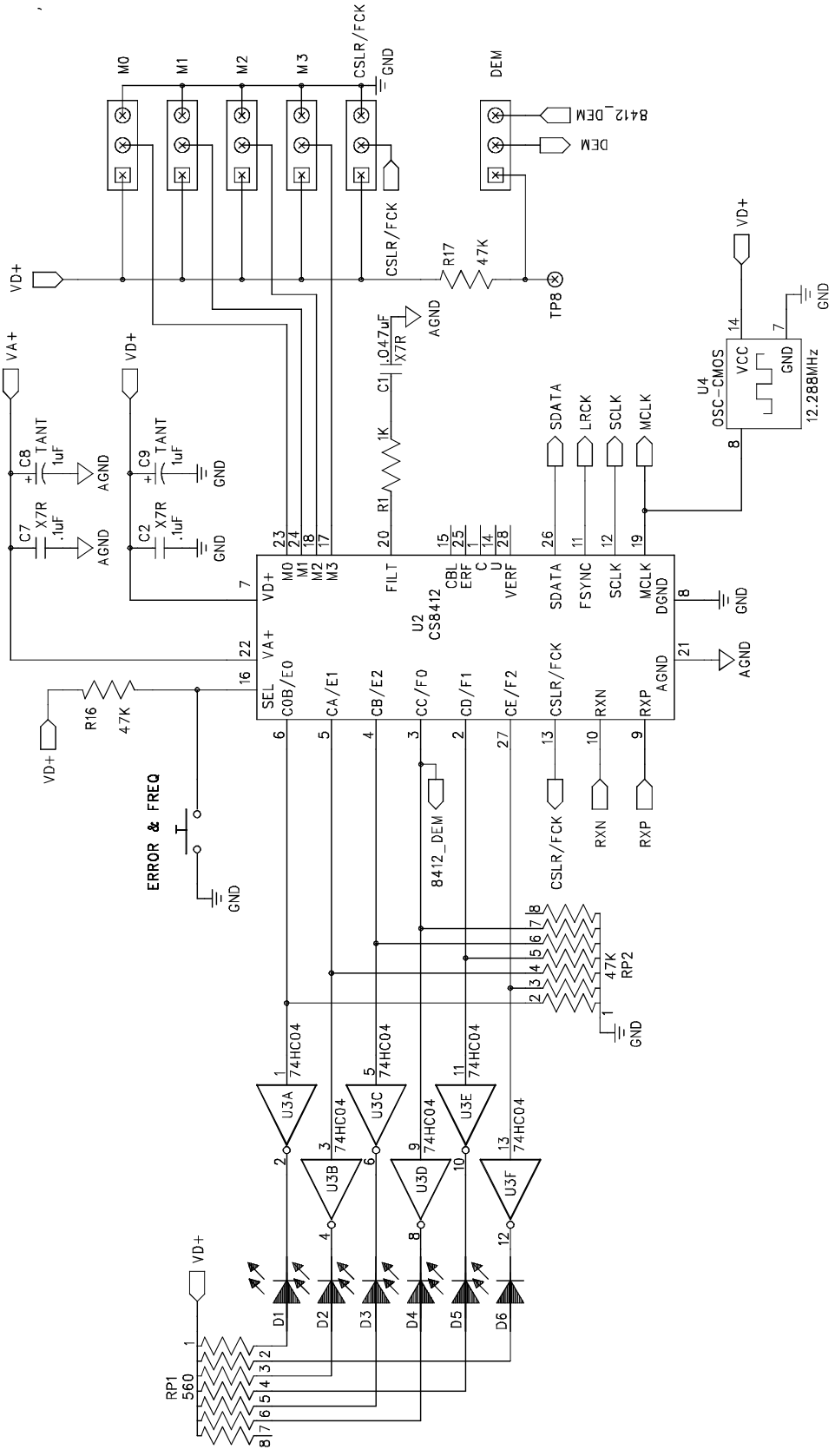


Figure 7. I/O Interface for Clocks and DATA



OPT1 Toshiba TORX173 optical receiver available from Insight Electronics

Figure 8. Digital Audio Input Circuit



Note: U2 and U4 can not be installed simultaneously

Figure 9. CS8412 and Connections

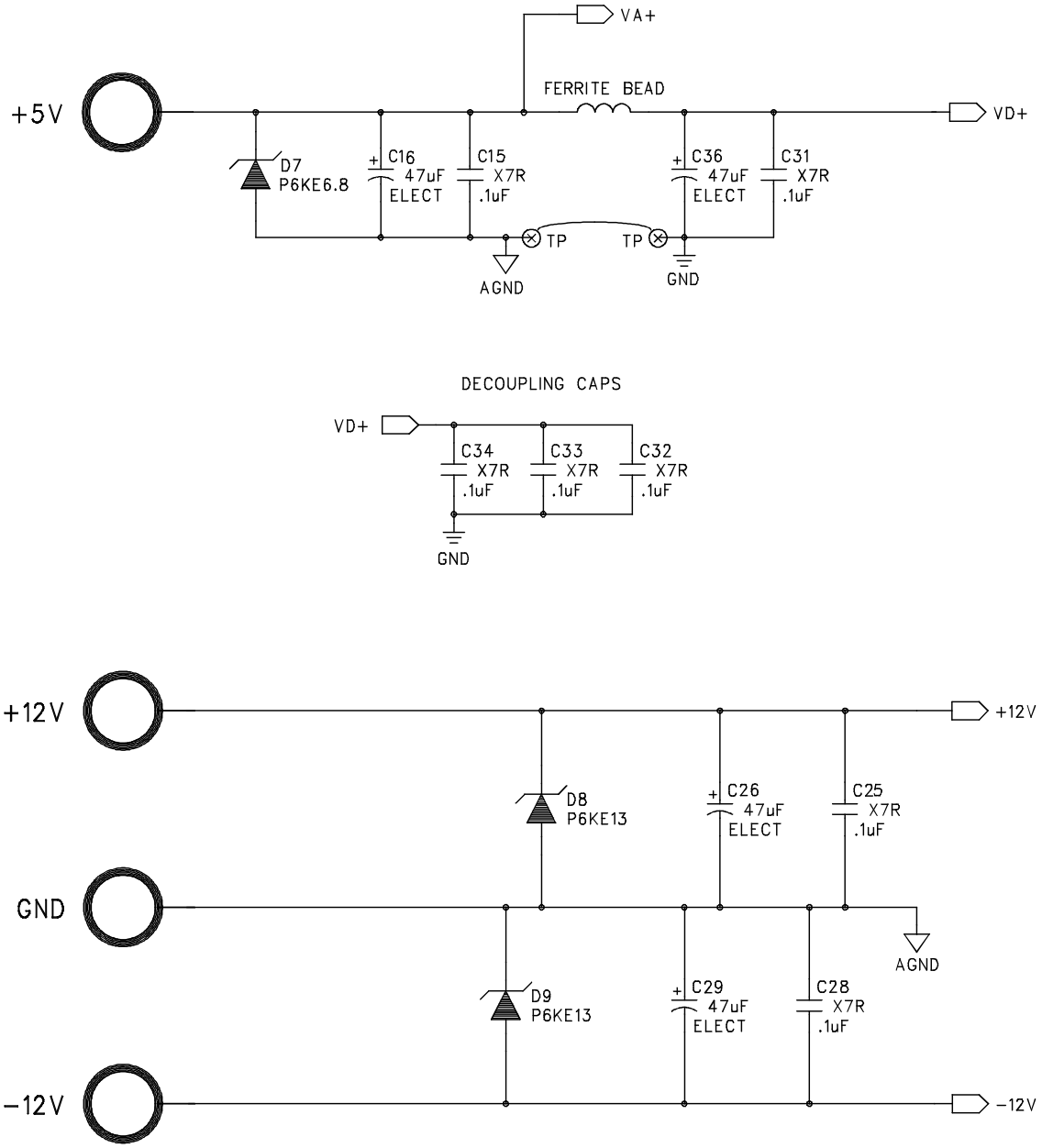


Figure 10. Power Supply Connections

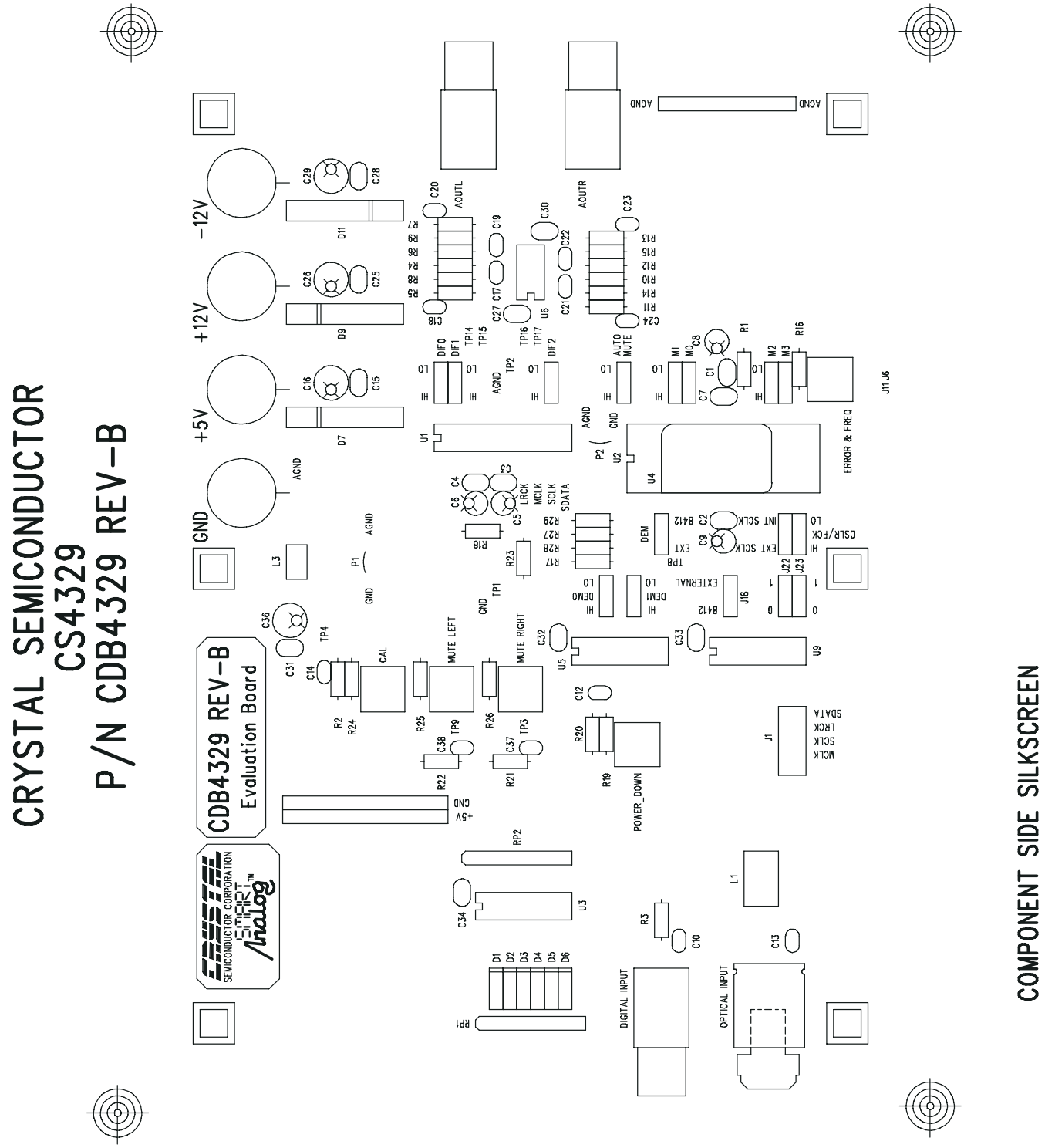


Figure 11. CDB4390 (CDB4329) Component Side Silkscreen

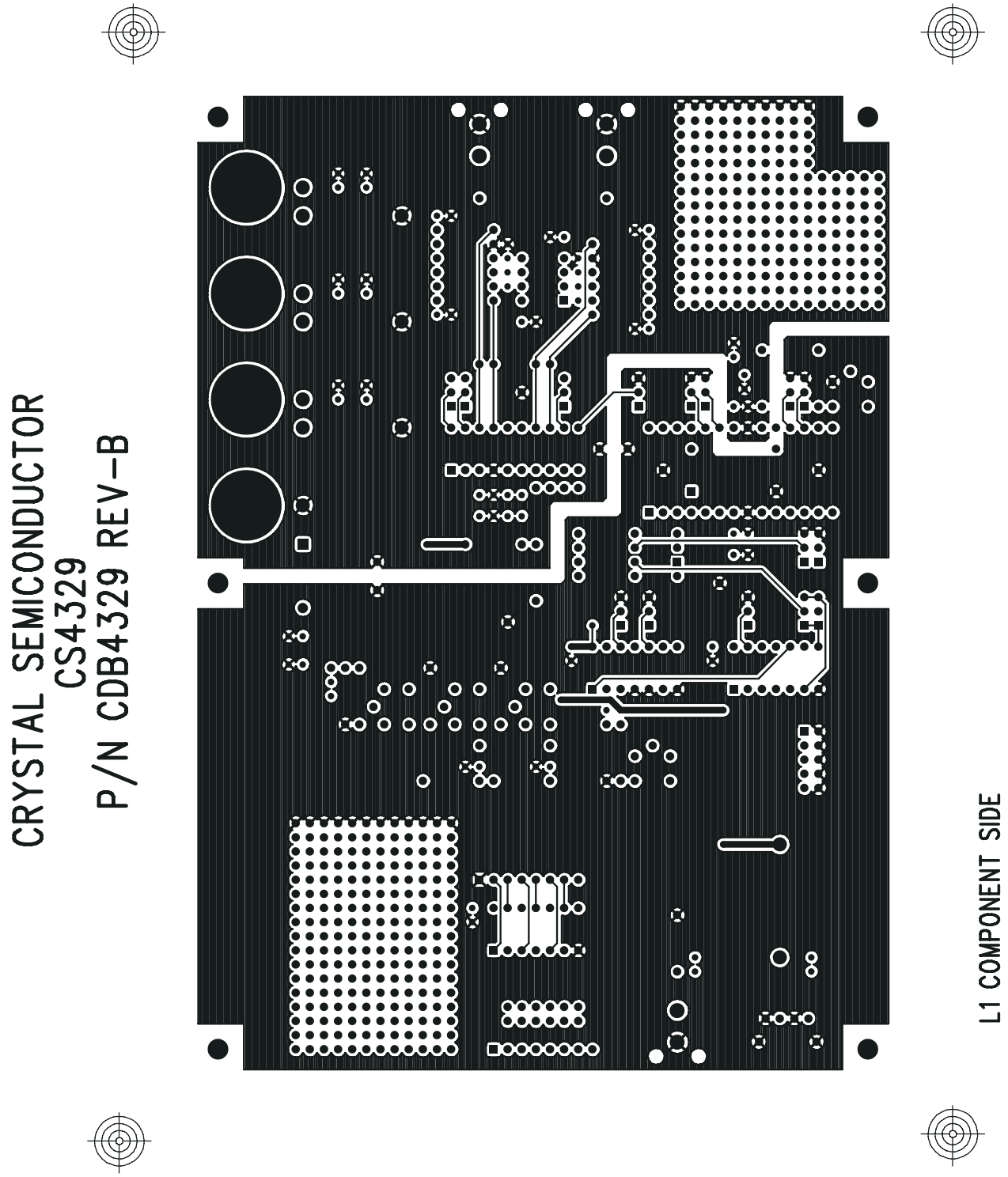


Figure 12. CDB4390 (CDB4329) Component Side (top)

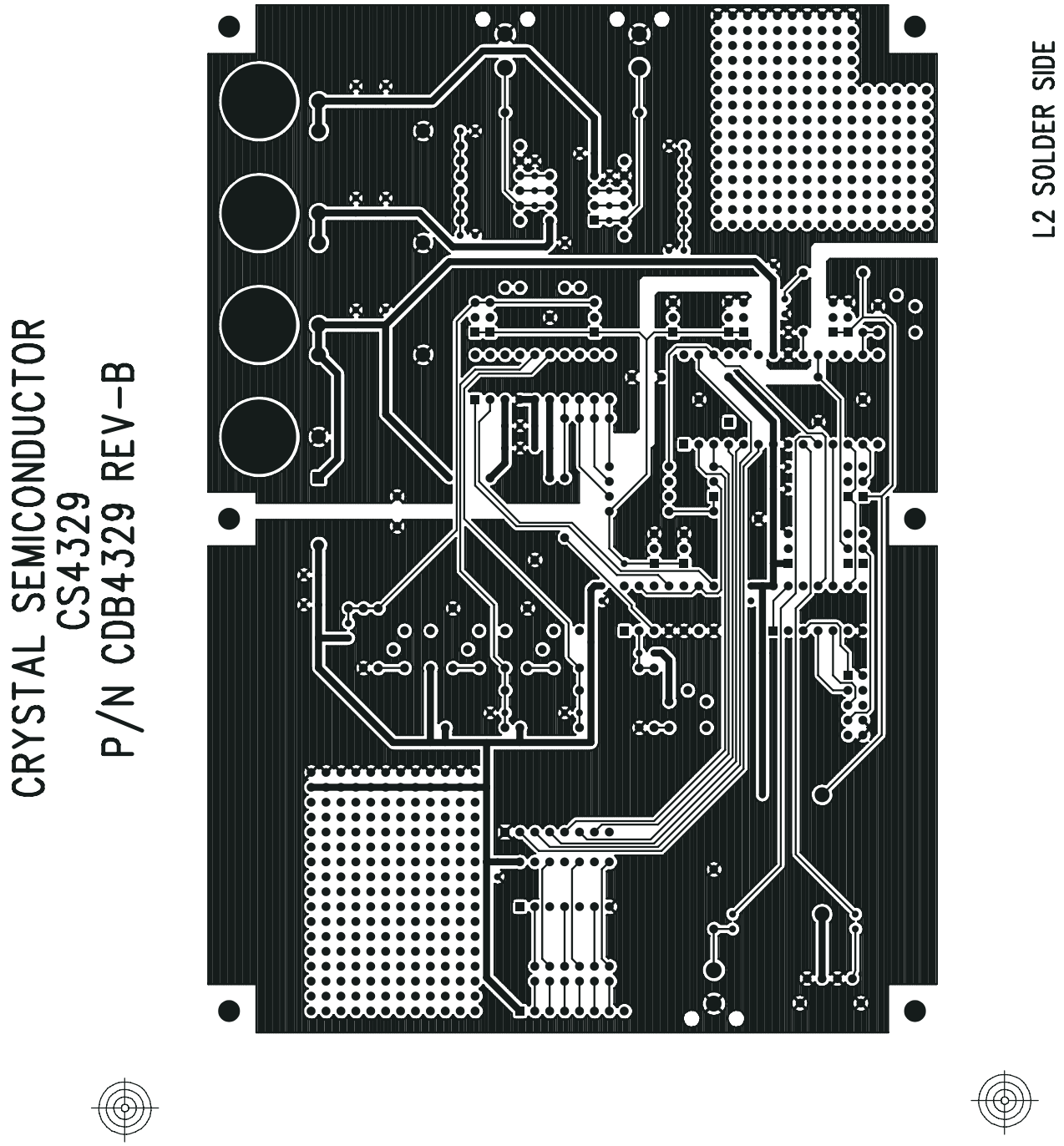


Figure 13. CDB4390 (CDB4329) Solder Side (bottom)

• Notes •